AMENDMENTS TO THE CLAIMS

Claim 1. (Currently Amended) An inspection method for simultaneously inspecting a plurality of semiconductor devices each having a respective input terminal for receiving an input signal, the method comprising:

preparing a first driver for outputting a signal to be used for inspection of a plurality of semiconductor devices;

connecting an output terminal of said first driver to a branching point;

connecting the respective input terminals of each of the plurality of semiconductor devices and the branching point through a current limiting element and a capacitor, said capacitor being connected in parallel to said current limiting element; [[and]]

outputting said signal from said first driver toward said branching point and;

preparing a second driver for outputting a signal to be used for inspection of a single device;

connecting an output terminal of the second driver to an input terminal of the single device and;

outputting the signal from the second driver toward the input terminal of the single device.

Claim 2. (Original) An inspection method according to claim 1, wherein a resistor is used as said current limiting element.

Claim 3. (Original) An inspection method according to claim 2, wherein resistance value of said resistor is set equal to or higher than 10 Ω.

Claim 4. (Original) An inspection method according to claim 1, wherein capacitance value of said capacitor is set equal to or higher than input capacitance value of the terminal to be connected.

Claim 5. (Original) An inspection method according to claim 1, wherein dc input resistance value of each of the terminals is equal to or higher than 0.1 MΩ.

Claim 6. (Original) An inspection method according to claim 1, wherein the semiconductor devices operate in synchronism with an external clock, and frequency of the external clock is equal to or higher than 10 MHz.

Claim 7. (Previously Presented) An inspection method for simultaneously inspecting a plurality of semiconductor devices each having a first terminal and a second terminal for receiving an input signal, the method comprising:

preparing a first driver for outputting a first signal to be used for inspection;

preparing a plurality of second drivers for outputting a second signal to be used for inspection;

connecting an output terminal of said first driver to a branching point;

connecting each of the first terminals of the semiconductor devices and the branching point through a current limiting element and a capacitor, said capacitor being connected in parallel to said current limiting element;

connecting output terminals of said plurality of second drivers and the second terminals to each other; and

outputting said first signal from said first driver toward said branching point and outputting said second signal from said plurality of second drivers to said second terminals.

Claim 8. (Original) An inspection method according to claim 7, wherein a resistor is used as said current limiting element.

Claim 9. (Original) An inspection method according to claim 8, wherein resistance value of said resistor is set equal to or higher than 10 Ω.

Claim 10. (Original) An inspection method according to claim 7, wherein capacitance value of said capacitor is set equal to or higher than input capacitance value of the terminal to be connected.

Claim 11. (Original) An inspection method according to claim 7, wherein dc input resistance value of each of the terminals is equal to or higher than 0.1 M Ω.

Claim 12. (Original) An inspection method according to claim 7, wherein the semiconductor devices operate in synchronism with an external clock, and frequency of the external clock is equal to or higher than 10 MHz.

Claim 13. (Original) An inspection method according to claim 12, wherein said external clock is supplied to the second terminals through the second drivers.

Claim 14. (Currently Amended) An inspection apparatus for simultaneously inspecting a plurality of semiconductor devices each having a

respective input terminal for receiving an input signal, the inspection apparatus comprising:

a first and second driver for outputting a signal to be used for inspection;

a branching point to which an output terminal of said first driver is connected;

a current limiting element interposed between each of the respective input terminals of the semiconductor devices and said branching point; [[and]]

a capacitor connected in parallel to each of the current limiting elements and

a connection between an output terminal of the second driver and an input of the semiconductor device not connected to the first driver.

Claim 15. (Original) An inspection apparatus according to claim 14, wherein said branching point, the current limiting elements and the capacitors are provided in a probe card or a test board for connecting semiconductor device to be inspected to a tester.

Claim 16. (Original) An inspection apparatus according to claim 14, wherein said current limiting element is a resistor.

Claim 17. (Original) An inspection apparatus according to claim 16, wherein resistance value of said resistor is equal to or higher than 10 Ω.

Claim 18. (Original) An inspection apparatus according to claim 14, wherein capacitance value of said capacitor is equal to or higher than input capacitance value of the terminal to be connected.

Claim 19. (Original) An inspection apparatus according to claim 14, wherein said current limiting element is a thermistor.

Claim 20. (Original) An inspection apparatus according to claim 14, wherein said current limiting element is a variable resistor, and said capacitor is a variable capacitor.

Claim 21. (Previously Presented) An inspection apparatus for simultaneously inspecting a plurality of semiconductor devices each having a first terminal and a second terminal for receiving an input signal, the inspection apparatus comprising of:

a first driver for outputting a first signal to be used for inspection;

a plurality of a second drivers for outputting a second signal to be used for inspection;

a branching point to which an output terminal of said first driver is connected;

a current limiting element interposed between the first terminals of the semiconductor devices and said branching point; and

a capacitor connected in parallel to said current limiting element;

wherein output terminals of said plurality of second drivers and the second terminals are connected to each other.

Claim 22. (Original) An inspection apparatus according to claim 21, wherein said branching point, the current limiting elements and the capacitors are provided in a probe card or a test board for connecting semiconductor device to be inspected to a tester.

Claim 23. (Original) An inspection apparatus according to claim 21, wherein said current limiting element is a resistor.

Claim 24. (Original) An inspection apparatus according to claim 22, wherein resistance value of said resistor is equal to or higher than 10 Ω.

Claim 25. (Original) An inspection apparatus according to claim 21, wherein capacitance value of said capacitor is equal to or higher than input capacitance value of the terminal to be connected.

Claim 26. (Original) An inspection apparatus according to claim 21, wherein said current limiting element is a thermistor.

Claim 27. (Original) An inspection apparatus according to claim 21, wherein said current limiting element is a variable resistor, and said capacitor is a variable capacitor.

Claim 28. (Original) An inspection apparatus according to claim 21, further comprising means for supplying a clock signal of a frequency equal to or higher than 10 MHz to said second terminals.

Claim 29. (Original) An inspection apparatus according to claim 21, wherein the second drivers supplies a clock signal of a frequency equal to or higher than 10 MHz to said second terminals.